REMARKS

The present amendment is in response to the *final* Office Action dated January 7, 2004, where the Examiner has rejected claims 1-34 and 58-71. By the present amendment, claims 1, 12, 23, 58, 70 and 71 have been amended. Accordingly, claims 1-34 and 58-71 are pending in the present application. Reconsideration and allowance of pending claims 1-34 and 58-71 in view of the amendments and the following remarks are respectfully requested.

A. Rejection of Claims 1-34 and 58-71 Under 35 USC §112, ¶ 1

The Examiner has rejected claims 1-34 and 58-71 under 35 USC §112, ¶ 1, as containing subject matter which was not described in the specification is such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

With respect to the Examiner's statement relating to the disclosure for "a substrate connected to a voltage" and "the pinned transfer gate being connected to the voltage", applicant has amended claim 1 to recite "substrate having a potential" and "the pinned transfer gate being pinned to the potential of the substrate." Applicant respectfully submits that the support for this amendment is found at, for example, page 6, line 12 - page 7, line 10. Further, independent claims 12, 23, 58, 70 and 71 have also been amended in a similar fashion.

The Examiner has also rejected claims 1-34 and 58-71 stating that "Applicant has not shown, nor is it known in the art, how to tie connect [sic] the "Pinned Transfer Gate" to the voltage of the substrate." In response to the Examiner's question, applicant respectfully submits that the teachings of Janesick 5,077,592 and other prior art references (mentioned below) can be used by one of ordinary skill in the art to manufacture the pinned transfer gate of the present application.

Applicant respectfully directs the Examiner's attention to a variety of patents and other references disclosing and teaching "pinned photodiodes", which illustrate that one of ordinary skill in the art could manufacture the pinned transfer gate of the present application at the time of filing of the present application.

Accordingly, applicant respectfully submits that the Examiner's rejection of claims 1-34 and 58-71 under 35 USC §112, ¶ 1, has been overcome.

B. Rejection of Claims 1-34 and 58-71 under the Judicially Created Doctrine of Obviousness-Type Double Patenting

The Examiner has rejected claims 1-34 and 58-71 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of co-pending Application Serial No. 09/977,444, assigned to the assignee of the present application, ESS Technology, Inc. Along with the present amendment, applicant has submitted a terminal disclaimer to overcome the Examiner's rejection under the judicially created doctrine of obviousness-type double patenting with respect to claim 1 of co-

pending Application Serial No. 09/977,444. Applicant respectfully submits that the enclosed terminal disclaimer overcomes the Examiner's rejection.

C. **Rejection of Claims 1-8 Under 35 USC §102 Claims 1 and 5-8**

The Examiner has rejected claims 1 and 5-8 under 35 USC §102(e) as being anticipated by U.S. patent application publication 2002/0121656 to Guidash ("Guidash '656"). For the reasons discussed below, applicant respectfully submits that the present invention, as defined by amended independent claim 1, is patentably distinguishable over Guidash '656.

Applicant respectfully submits that the present invention, as defined by amended independent claim 1, is directed to "an imager cell including a substrate having a potential," wherein the imager cell comprises "a photoreceptor; a sense node; and a pinned transfer gate disposed between the photoreceptor and the sense node, the pinned transfer gate being pinned to the potential of the substrate and further being configured transfer charge between the photoreceptor and the sense node." As discussed in the present application, a "pinned transfer gate" is tied or pinned to the same voltage or potential as the substrate. For example, the pinned transfer gate and the substrate may both be connected to ground or zero volts. See, for example, page 7, lines 6-7 of the present application. As a result, this arrangement of the imager cell of claim 1 eliminates the need for a transistor gate structure, which is conventionally used to transfer charge

from the photoreceptor to the sense node. Further, it is respectfully submitted that pinning the transfer gate generally suppresses dark current, which leads to an improved signal to noise ratio because fewer dark current electrons (i.e., noise electrons) contribute to the output signal

Applicant respectfully submits that in view of the Examiner's response to applicant's argument, applicant has amended claim 1 to recite that "the pinned transfer gate being pinned to the potential of the substrate." Applicant further notes that the teachings of Janesick 5,077,592 and a variety of patents and other references, which disclose and teach "pinned photodiodes", further clarify the above distinction between claim 1 and Guidash.

To clarify the readout operation of the present invention, applicant references the potential well diagram 214 of Figure 2 and the description set forth beginning on page 8, line 7 of the present application, wherein the specification describes that "after integration period 222, the control circuitry 114 applies the readout voltage V- to establish the readout potential well 228. Note that the readout potential well 228 is shallower than the transfer potential well 230, established by pinned transfer gate 206. As a result, electrons captured by the integration potential well 226 propagate through the transfer potential well 230 and into the sense node potential well." As pointed out above, this readout operation is achieved without requiring a transistor gate structure for the pinned transfer

gate due to the unique structural arrangement employing pinned transfer gate 206, which is tied to the same potential as substrate 202 in Figure 2.

In contrast, the disclosure of Guidash '656 fails to disclose or remotely suggest a pinned transfer gate as specified by claim 1. For example, with reference to Figures 2 and 5 of Guidash '656, charge is transferred from photodiode 12 to sense node 24 by way of transfer transistor 14 (Figure 2 of Guidash '656) corresponding to transfer transistor structure 16 (Figure 5 of Guidash '656). As clearly shown in Figure 5 of Guidash '656, transfer transistor 14, by its nature, includes a transistor gate structure situated between source and drain regions 34. As such, transfer transistor 14 cannot be a pinned transfer gate as specified by claim 1, because, a pinned transfer gate does not include a transistor gate structure, as discussed above. Moreover, the gate of transfer transistor 14 (labeled "TG" in Figure 2 of Guidash '656) is not tied to the same potential as the substrate in Guidash '656. Instead, in order transfer charge from photodiode 12 to sense node 24 in Guidash '656, a sufficient voltage would need to be supplied to the gate of the transfer transistor 14 to turn on transfer transistor 14. In sum, Guidash '656 simply discloses a typical transfer transistor arrangement employing a transistor gate structure for transferring charge from photodiode 12 to sense node 24, and neither discloses nor remotely suggests the pinned transfer gate specified by claim 1. For these reasons, applicant respectfully submits that the rejection of independent claim 1 and its

corresponding dependent claims 2-11 has been traversed, and that, therefore, claims 1-11 should now be allowed.

The Examiner has rejected claims 1-6 under 35 USC §102(e) as being anticipated by U.S. patent application publication 2002/0121655 to Zheng, et al. ("Zheng '655"). For the reasons discussed below, applicant respectfully submits that the present invention, as defined by amended independent claim 1, is patentably distinguishable over Zheng '655.

With respect to Figure 1 of Zheng '655, a transistor (identified as "p-MOSFET" in Zheng '655) is used to transfer charge collected by photodiode 22. As such, p-MOSFET includes a transistor gate structure (shown but not designated with a reference number in Figure 1 of Zheng '655) situated between source and drain regions of the p-MOSFET. For similar reasons discussed above in conjunction with Guidash '655, p-MOSFET shown in Figure 1 of Zheng '655 cannot be a pinned transfer gate as specified by claim 1, since it includes a transistor gate structure, which must be enabled to transfer charge from photodiode 22 to a sense node.

Similarly, with respect to Figure 5 of Zheng '655, SIO transistor 83, functioning as a transfer transistor, includes a transistor gate structure (shown but not designated with a reference number in Figure 5 of Zheng '655) situated between source and drain regions. As such, silicon-on-insulator ("SIO") transistor 83 cannot be a pinned transfer gate as specified by claim 1, since it includes a transistor gate structure, which must be enabled to transfer charge from photo-collection area 98 to sense node 96.

Furthermore, neither are the transistor gate structures of p-MOSFET shown in Figure 1 of Zheng '655 and/or SIO transistor 83 shown in Figure 5 of Zheng '655 connected to the same voltage as the substrate. In sum, Zheng '655 simply discloses a typical transfer transistor arrangement employing a transistor gate structure for transferring charge from a photodiode to a sense node, and neither discloses nor remotely suggests the pinned transfer gate specified by claim 1. For these reasons, applicant respectfully submits that the rejection of independent claim 1 and its corresponding dependent claims 2-11 has been traversed, and that, therefore, claims 1-11 should now be allowed.

D. Rejection of Claims 9-34 and 58-71 Under 35 USC §103 Claim 9-11.

The Examiner has rejected dependent claims 9-11 under 35 USC §103(a) as being unpatentable over Zheng '655 in view of Turko, et al. (USPN 5,121,214) ("Turko '214"). As discussed above, independent claim 1 is patentably distinguishable over Zheng '655 and, as such, claims 9-11 depending from independent claim 1, are, a fortiori, also patentably distinguishable over Zheng '655. Accordingly, claims 9-11 are patentably distinguishable over Zheng '655 in view of Turko '214.

The Examiner has rejected claims 12-34 and 58-71 under 35 USC §103(a) as being unpatentable over Guidash '656. Applicant respectfully disagrees; however, in order to expedite the prosecution of the present application, applicant has amended independent

claims 12, 23, 58, 70 and 71 to specify limitations analogous to those specified by independent claim 1. As discussed above, independent claim 1 is patentably distinguishable over Guidash '656. Accordingly, applicant respectfully submits that independent claims 12, 23, 58, 70 and 71, and their corresponding dependent claims 13-22, 24-34 and 59-69 are allowable over Guidash '656 for at least the same reasons claim 1 is allowable over Guidash '656, as discussed above.

The Examiner has rejected claims 12-34 and 58-71 under 35 USC §103(a) as being unpatentable over Zheng '655. Applicant respectfully disagrees; however, in order to expedite the prosecution of the present application, applicant has amended independent claims 12, 23, 58, 70 and 71 to specify limitations analogous to those specified by independent claim 1. As discussed above, independent claim 1 is patentably distinguishable over Zheng '655. Accordingly, applicant respectfully submits that independent claims 12, 23, 58, 70 and 71, and their corresponding dependent claims 13-22, 24-34 and 59-69 are allowable over Zheng '655 for at least the same reasons claim 1 is allowable over Zheng '655, as discussed above.

E. Conclusion

For all the foregoing reasons, an early allowance of claims 1-34 and 58-71 pending in the present application is respectfully requested.

Respectfully Submitted;
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